R E M A R K S

Careful review and examination of the subject application are noted and appreciated.

SUPPORT FOR CLAIM AMENDMENTS

Support for the amendments to the claims can be found in the drawings as originally filed, for example, on FIGS. 3, 6 and 7 and in the specification as originally filed, for example, on page 7, line 5 through page 8, line 2. As such, no new matter has been introduced.

CLAIM REJECTIONS UNDER 35 U.S.C. §102

The rejection of claims 1, 4, 5, 8-10, 13-15, 18 and 19 under 35 U.S.C. §102(b) as being anticipated by Hardin (U.S. patent No. 5,631,920; hereinafter Hardin '920) is respectfully traversed and should be withdrawn.

Hardin '920 is directed to a spread spectrum clock generator (Title). The clock generator circuits are digital and may be reset to a starting condition to synchronize the spread spectrum clock (Abstract).

In contrast to Hardin '920, the presently claimed invention (claim 1) provides that the spread spectrum **modulation** of the clock signal is **switched on** in response to a first state of a command signal and **switched off** in response to a second state of

the command signal. Claims 13 and 14 include similar limitations. Hardin '920 does not disclose or suggest a command signal that switches on spread spectrum modulation when in a first state and switches off spread spectrum modulation when in a second state. Therefore, Hardin '920 does not disclose or suggest each and every element of the presently claimed invention, arranged as in the present claims. As such, the presently claimed invention is fully patentable over Hardin '920 and the rejection should be withdrawn.

Specifically, assuming *arguendo*, the elements 50-60 of FIG. 7 of Hardin '920 are similar to the presently claimed first circuit, the signal 68 in FIG. 7 of Hardin '920 is similar to the presently claimed clock signal, the signal 50 in FIG. 7 of Hardin '920 is similar to the presently claimed reference signal, the element 56 in FIG. 7 of Hardin '920 is similar to the presently claimed sequence of spread spectrum ROM codes and the element 54 in FIG. 7 of Hardin '920 is similar to the presently claimed command signal (as suggested in section 3, lines 3-18 of the Office Action and for which Applicants' representative does not necessarily agree), Hardin '920 fails to disclose or suggest the spread spectrum modulation of a clock signal is switched on in response to a first state of the reset signal 54 and switched off in response to a second state of the reset signal 54. In particular, the signal 54 of Hardin '920 provides synchronization of a spread spectrum clock to the same point in the spread spectrum for each

sweep of a device (e.g., a laser printer) using the clock (see column 8, lines 29-37 of Hardin '920). Since the signal 54 of Hardin '920 does not switch on the spread spectrum modulation when in a first state and switch off the spread spectrum modulation when in a second state, Hardin '920 fails to disclose or suggest each and every element of the presently claimed invention, arranged as in the present claims. As such, the presently claimed invention is fully patentable over the cited reference and the rejection should be withdrawn.

Claims 2-12 and 15-20 depend, either directly or indirectly, from claim 1 or claim 14 which are believed to be allowable. As such, the presently claimed invention is fully patentable over the cited reference and the rejection should be withdrawn.

New claims 22-25 depend, either directly or indirectly, from claims 1, 14 or 21 which are believed to be allowable. As such, the presently claimed invention is fully patentable over the cited reference.

CLAIM REJECTIONS UNDER 35 U.S.C. §103

The rejection of claims 6, 7 and 20 under 35 U.S.C. §103(a) as being unpatentable over Hardin '920 in view of Marten et al. (U.S. Patent No. 6,590,949; hereinafter Marten) is respectfully traversed and should be withdrawn.

The rejection of claims 11, 12 and 21 under 35 U.S.C. §103(a) as being unpatentable over Hardin '920 in view of Hardin et al., design consideration of phase-locked loop systems for spread spectrum clock generation capability, IEEE 1997 IS on EC, August 19-22, 1997, pp. 302-307 (hereinafter Hardin IEEE) is respectfully traversed and should be withdrawn.

The rejection of claims 16 and 17 under 35 U.S.C. §103(a) as being unpatentable over Hardin '920 as applied to claim 15, and further in view of Hardin IEEE and Young et al., A PLL Clock Generator with 5 to 110 MHz of Lock Range for Microprocessors, IEEE Journal of Solid-State Circuits, Vol. 27, Issue 11, Nov. 1992, pp. 1599-1607 (hereinafter Young) is respectfully traversed and should be withdrawn.

Claims 6, 7, 11, 12, 16, 17, and 20 depend, directly or indirectly, from either claim 1 or claim 14 which are believed to be allowable. As such, the presently claimed invention is fully patentable over the cited references and the rejections should be withdrawn.

With respect to claim 21, contrary to the position taken in the Office Action on pages 5, line 19 through page 6, line 3, that Hardin '920 discloses a second circuit/means configured to synchronize the command signal (element 54 of Hardin '920) to a feedback signal (element 68 of Hardin '920), both Hardin '920 and Hardin IEEE appear silent regarding a second circuit configured to

synchronize a command signal to a feedback signal, as presently claimed. Specifically, assuming *arguendo*, the signal 54 is similar to the presently claimed command signal and the signal 68 is similar to the presently claimed feedback signal (as suggested on page 6, lines 1-3 of the Office Action and for which Applicants' representative does not necessarily agree), Hardin '920 fails to teach or suggest that the signal 54 is in any way synchronized to the signal 68. Rather, Hardin '920 states that the signal 54 is used to synchronize the signal 68 to certain events (e.g., sweep in a laser printer) in an application. For example, in column 8, lines 29-37, Hardin recites that clock times may be in a spread spectrum without significant degradation of the printing if each sweep is synchronized to the same point in the spread spectrum. Hardin further recites that the reset input on line 54 provides such a synchronization (column 8, line 38 of Hardin '920). Since the signal 54 is used to synchronize the signal 68 to application events, it follows that Hardin '920 and Hardin IEEE, alone or in combination, do not teach or suggest a second circuit configured to synchronize the command signal to a feedback signal, as presently claimed. As such, the presently pending claim 21 is fully patentable over the cited references and the rejection should be withdrawn.

Accordingly, the present application is in condition for allowance. Early and favorable action by the Examiner is

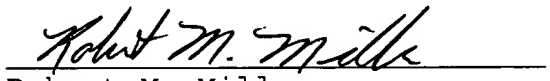
respectfully solicited.

The Examiner is respectfully invited to call the Applicants' representative should it be deemed beneficial to further advance prosecution of the application.

If any additional fees are due, please charge our office Account No. 50-0541.

Respectfully submitted,

CHRISTOPHER P. MAIORANA, P.C.



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